Remarks

Claims 47-67 are pending in this application. Claims 64 and 65 are rejected. Claims 47-63, 66, and 67 are withdrawn from consideration. Claims 1-46 have previously been cancelled.

New claims 68-69 are presented for examination.

Claim Rejections – 35 USC § 102

Claim 64 is rejected under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over *Barth et al.* (US 2002/0076917).

Applicants respectfully traverse the present rejection for the following reasons. The amended claims specify that the claimed wafer comprises a **silicon** wafer substrate. Support for this amendment can be found on page 3, line 10 of the Specification. In addition, claims 66 and 67 refer to p-type or n-type silicon forming the silicon wafer substrate. Support for this is found on page 3, line 11.

Barth et al. (US2002/0076917 A1) disclose a metallization insulating structure which is shown in Figure 2 and Figure 3 of that reference. The structure comprises a capping layer 20, a first undoped insulator 10 and a second doped insulating material 15 (*Barth et al.,* paragraphs [0024] and [0028]).

Barth et al. distinguishes between the first undoped insulator 10 and the second doped insulating material 15. Nevertheless, the Examiner alleges that insulating material 15 would read on the high stress LPPECVD-LTO layer which is claimed in claim 64. The assertion by the Examiner is wrong, since insulating material 15 does not consist of oxide but of **doped** oxide. Insulator 10 and insulating material 15 are distinguishable by chemical analysis. In contrast, both the claimed high stress LPPECVD-LTO layer and the claimed low stress LPPECVD-LTO layer are oxide layers and do not differ from each other in terms of their chemical components.

Adding a dopant to one of the oxide layers as suggested by *Barth et al.* and formally not excluded by the "comprising" wording in claim 64 would lead to a two layer back side seal comprising an oxide layer and a **doped** oxide layer, i.e. to something different than that which is actually claimed in claim 64.

The capping layer 20 of *Barth et al.* consists of material such as silicon nitride, silicon carbide or hydrogenated silicon carbide (cf. [0025]). Thus, layer 20 certainly does not read on the silicon wafer substrate 1 claimed in claim 64. It is noted that *Barth et al.* discloses the capping layer as being preferred, only (see *Barth et al.* paragraph [0024]). However, it is noted also that *Barth et al.* is completely silent about a specific substrate.

Accordingly, for at least these reasons claims 64 is allowable under 35 U.S.C. § 102(b) or, in the alternative, under 35 U.S.C. § 103(a) over *Barth et al.*

Claim Rejections – 35 USC § 103

Claim 65 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Barth et al.* (US 2002/0076917) as applied to claim 64 above, in view of *Chen et al.* (US 6,440,840).

Applicants respectfully traverse the present rejection for the following reasons. Claim 65 is allowable since it depends from claim 64 which is shown above to be allowable.

Notwithstanding the allowablilty of claim 65 via its dependence from claim 64, claim 65 is independently allowable. The deficiencies of *Barth et al.* are set forth above. The Examiner refers to Chen et al. (US 6,440,840 B1) which teaches a similar structure as *Barth et al.* This structure necessarily includes a barrier layer 12 which consists of silicon nitride (*Chen et al.,* col. 4, line 6). The barrier layer 12 reads on the capping layer 20 of *Barth et al.* which is also preferably made of silicon nitride (*Barth et al.*, [0025]). *Chen et al.* teaches the deposition of an insulating layer 14 on the barrier layer 12 (*Chen et al.*, col. 4. line 12) whereas *Barth et al.* teaches to deposit an undoped first insulating layer 10 on the capping layer 20 (*Barth et al.*,

Figures 2 and 3). Therefore, the combined teachings of *Barth, et al.* and *Chen et al.* are silent with respect to depositing a low stress LPPECVD-LTO layer on a silicon wafer substrate as claimed in claim 64. Moreover, *Chen et al.* teaches away from depositing a low stress LPPECVD-LTO layer on a silicon wafer substrate since the structure disclosed in that reference requires that the insulating layer be deposited on a barrier layer. Therefore, the wafer claimed in the amended claims is not obvious over the combination of *Barth et al.* and *Chen et al.*

Accordingly, for at least these reasons claim 65 is allowable under 35 U.S.C. § 103(a) over *Barth et al.,* in view of *Chen et al.*

Conclusion

Applicants have made a genuine effort to respond to each of the Examiner's objections and rejections in advancing the prosecution of this case. Applicants believe that all formal and substantive requirements for patentability have been met and that this case is in condition for allowance, which action is respectfully requested. If any additional issues need to be resolved, the Examiner is invited to contact the undersigned at his earliest convenience.

Please charge any fees or credit any overpayments as a result of the filing of this paper to our Deposit Account No. 02-3978.

Respectfully submitted,

Jin-Xing Li et al.

By: /James W. Proscia/
James W. Proscia, Reg. No. 47,010
Attorney/Agent for Applicant

Date: February 23, 2011

BROOKS KUSHMAN P.C.
1000 Town Center, 22nd Floor
Southfield, MI 48075-1238
Phone: 248-358-4400
Fax: 248-358-3351